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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,050	09/30/2003	Zenko Gergintschew	WMP-IFT-823	5870

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,050	GERGINTSCHEW, ZENKO	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 11/18/2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's acknowledged prior art.

With respect to claim 1, applicant's acknowledged prior art [Fig. 1 and Fig. 2A-2B] teaches a method for driving a semiconductor switch [Fig. 1, T] having load current limiting [Fig. 1, Current Sensor 2] and thermal protection [Fig. 1, Temperature Sensor 1), a maximum load current being limited and the semiconductor switch [Fig. 1, T] switching off upon a predetermined upper temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tso] being exceeded and switching on again when a chip temperature falls below a predetermined lower temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tsu; applicant's specifications page 11, lines 18-26 and Fig. 2A], which comprises the steps of operating the semiconductor switch in one of a normal mode [Fig. 1, The semiconductor switch T is in a normal mode when the chip temperature falls below a given lower chip temperature, or when the switch T is on] and a fault mode [Fig. 1, The semiconductor switch T is in a fault mode when the chip temperature exceeds an upper temperature value, or when the switch T is off]; operating the semiconductor switch in the fault mode upon exceeding the predetermined upper temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tso] as disclosed in applicant's specifications, page 11, lines 18-20]; and limiting a load current to a first maximum value [Fig. 2B, Ids1] in

the normal mode and to a second maximum value [Fig. 2B, when Ids is zero], being lower than the first maximum value [Fig. 2B, Ids1], in the fault mode.

With respect to claim 2, applicant's prior art teaches that the method further comprises switching on the semiconductor switch T when the chip temperature falls below the predetermined lower temperature Tsu in the normal mode and in the fault mode as disclosed in specifications page 11, lines 18-26 and Fig. 2A [The transistor switch T is on at the crossing point between the fault mode and normal mode as seen by the intersection of the chip temperature crossing Tsu (Fig. 2B) on its way down when compared to the corresponding current of Fig. 2B].

With respect to claim 4, applicant's prior art teaches that the method further comprises limiting the load current by actuating the semiconductor switch [Fig. 1, T].

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Busick et al., Patent No. 5,373,205.

With respect to claim 1, Busick teaches a method for driving a semiconductor switch having load current limiting and thermal protection [Col. 1, lines 7-10], a maximum load current being limited and the semiconductor switch [Fig. 1, 16] switching off [Off-time duty cycle is increased; col. 5, lines 52-56; col. 6, lines 17-60] upon a predetermined upper temperature being exceeded [col. 3, lines 14-17] and switching on again when a chip temperature falls below a predetermined lower temperature [col. 3, lines 17-20], which comprises the steps

of operating the semiconductor switch in one of a normal mode [Peak current mode] and a fault mode [nominal current mode]; operating the semiconductor switch in the fault mode upon exceeding the predetermined upper temperature; and limiting a load current to a first maximum value in the normal mode [Fig. 3, steps 418, 421] and to a second maximum value, being lower than the first maximum value, in the fault mode [Fig. 3, step 420].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's acknowledged prior art, in view of Thomas, Patent No. 6,052,268.

Applicant's acknowledged prior art does not disclose that the method further comprises monitoring a voltage across a load path of the semiconductor switch; and operating the semiconductor switch in the normal when a load path voltage is smaller than a predetermined threshold value.

Thomas teaches an electrical apparatus which comprises a semiconductor-switching device 3 and a voltage sensing device 5 to monitor a voltage across a load path of the semiconductor switch 3 as disclosed in Col. 2, lines 30-33 and Fig. 1.

Both teachings are related by being semiconductor switches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Thomas, which teaches a method of calculating power dissipation through a semiconductor switch using voltage and current sensors, along with the applicant's acknowledged prior art because during overload conditions, current flow along with power dissipation increases dramatically through a transistor. Taken together, Thomas's method of measuring power dissipation can be combined with the method of switching between two operating levels to produce the applicant's method of detecting overvoltage, to more accurately measure current flow.

Allowable Subject Matter

4. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 3: The prior art does not disclose that the method further comprises switching off the semiconductor switch, when in the fault mode, if a further upper temperature is exceeded, the further upper temperature is lower than the predetermined upper temperature.

Claims 6-8 are allowed.

The following is an examiner's statement of reasons for indicating allowance of claim 6: The prior art does not disclose a protective circuit storing

first and second overcurrent signals, said protective circuit assuming one of a first operating mode and a second operating mode, and, depending on a mode, said protective circuit controlling said semiconductor switch according to a comparison of the current measuring signal to the first overcurrent signal or according to a comparison of the current measuring signal to the second overcurrent signal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
02/27/2007

BRIAN SIRCUS
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